Physics Based Reliability Qualification using fiXtress

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VISION

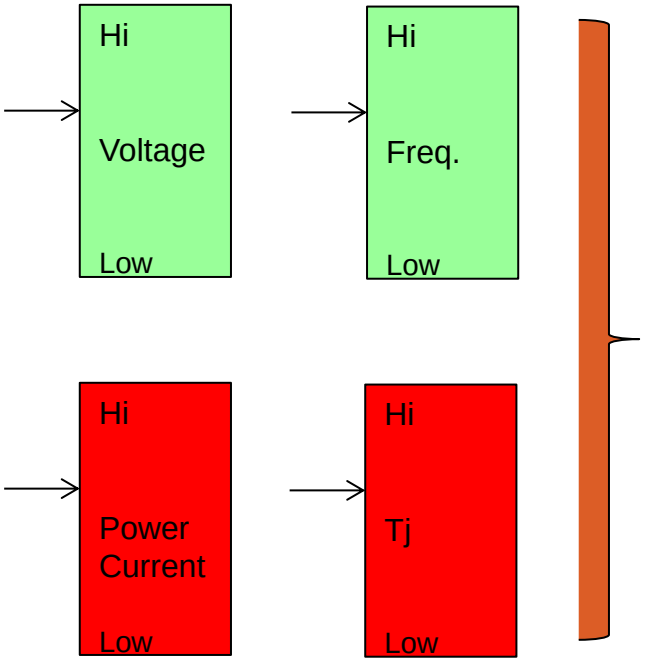
- To make a state-of-the-art bridge from Academic Research to sophisticated Industrial needs in the area of Failure Analysis and Reliability
- To take the reliability knowledge of Electronics Industry directly to the users of nano-scale and VLSI Circuits

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- How to make Accurate Predictions
- FIT Rate calculation today
- Limitation of HTOL and single mechanism model
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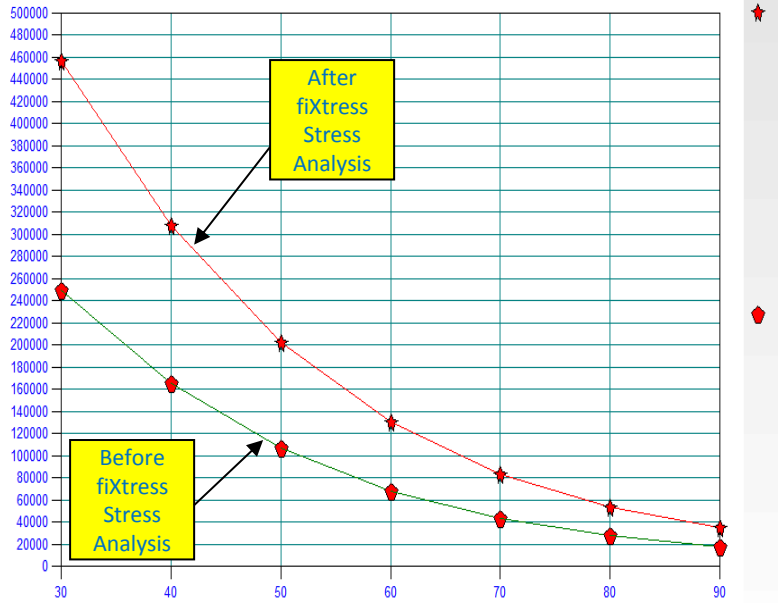
The connection to fiXtress

New tool based on 4 stress parameters



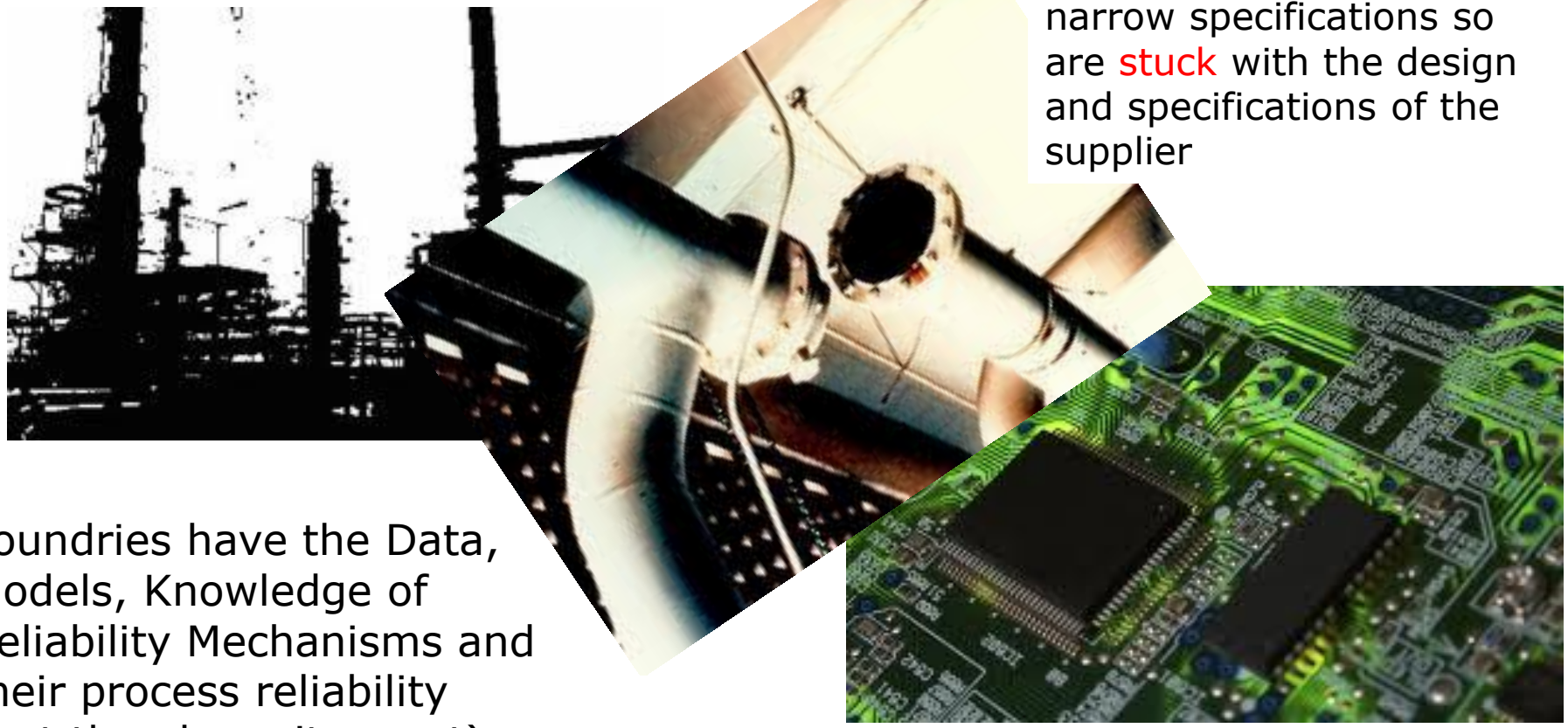
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MTBF



Fix the Broken Pipe with FIXtress™

Chip Manufacturers specify parameters based on Foundry's Models

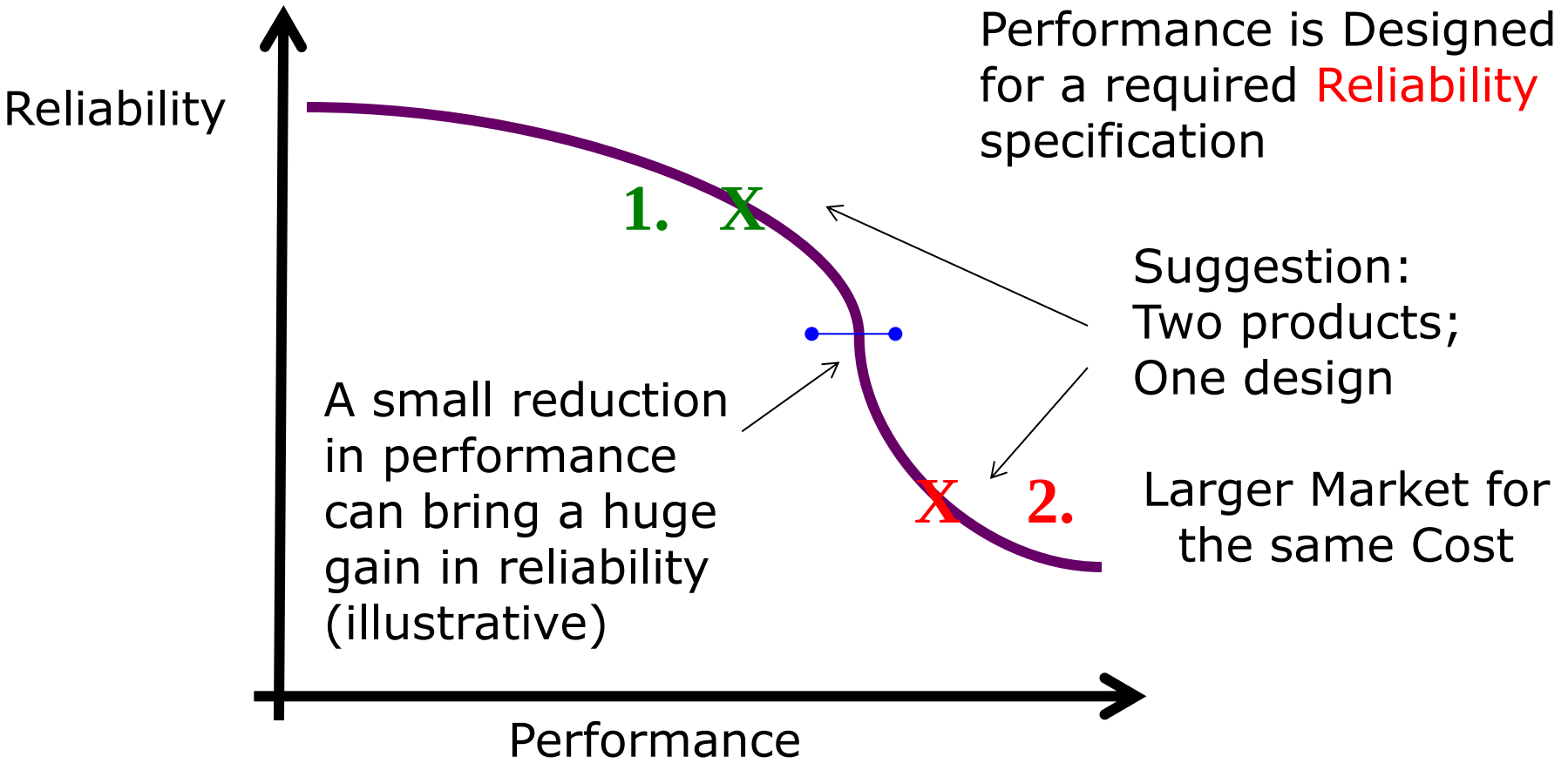


Customers who build boards are bound by narrow specifications so are stuck with the design and specifications of the supplier

Foundries have the Data, Models, Knowledge of Reliability Mechanisms and their process reliability (but they keep it secret)

Benefit to the Supplier !!

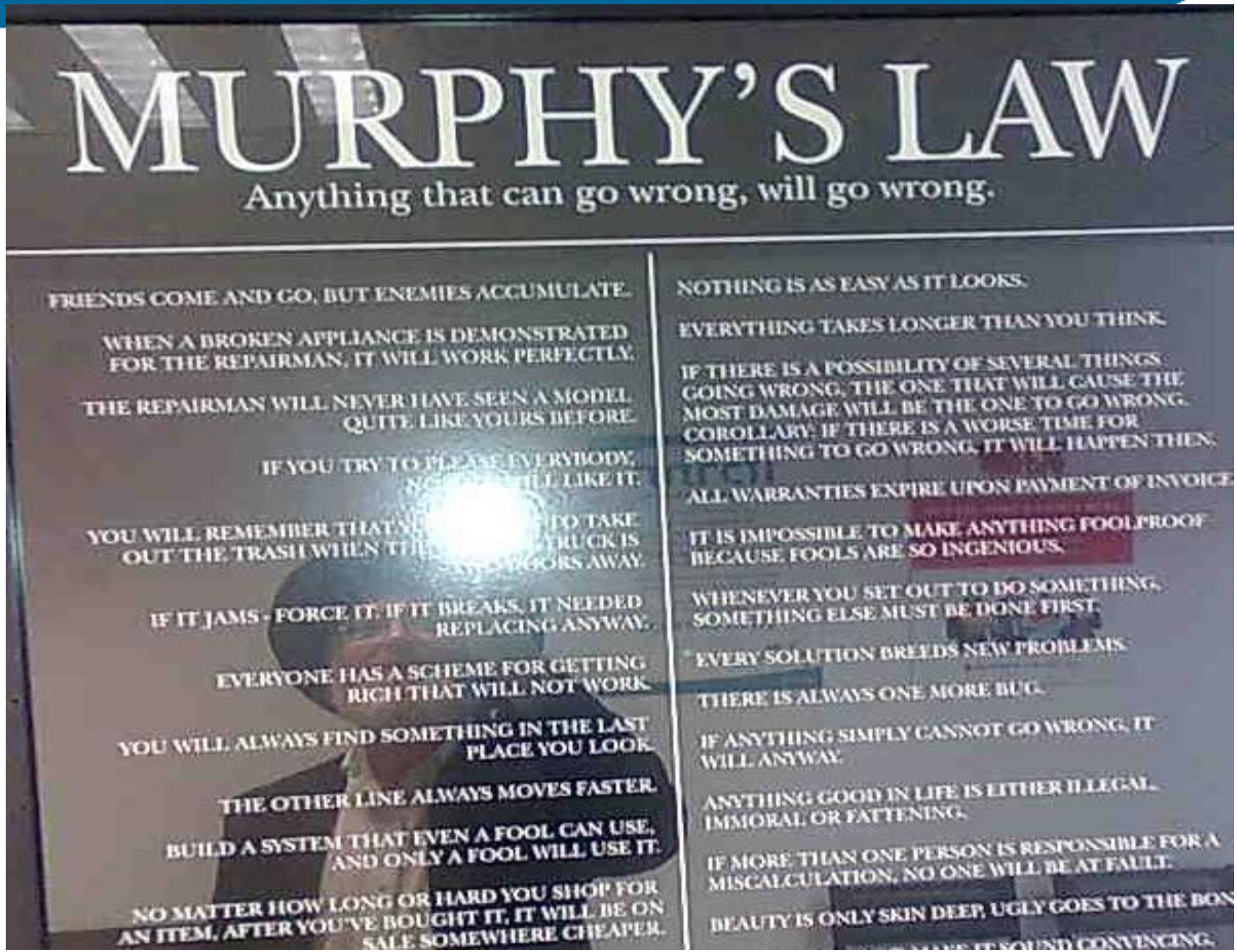
More applications means **more Sale$**



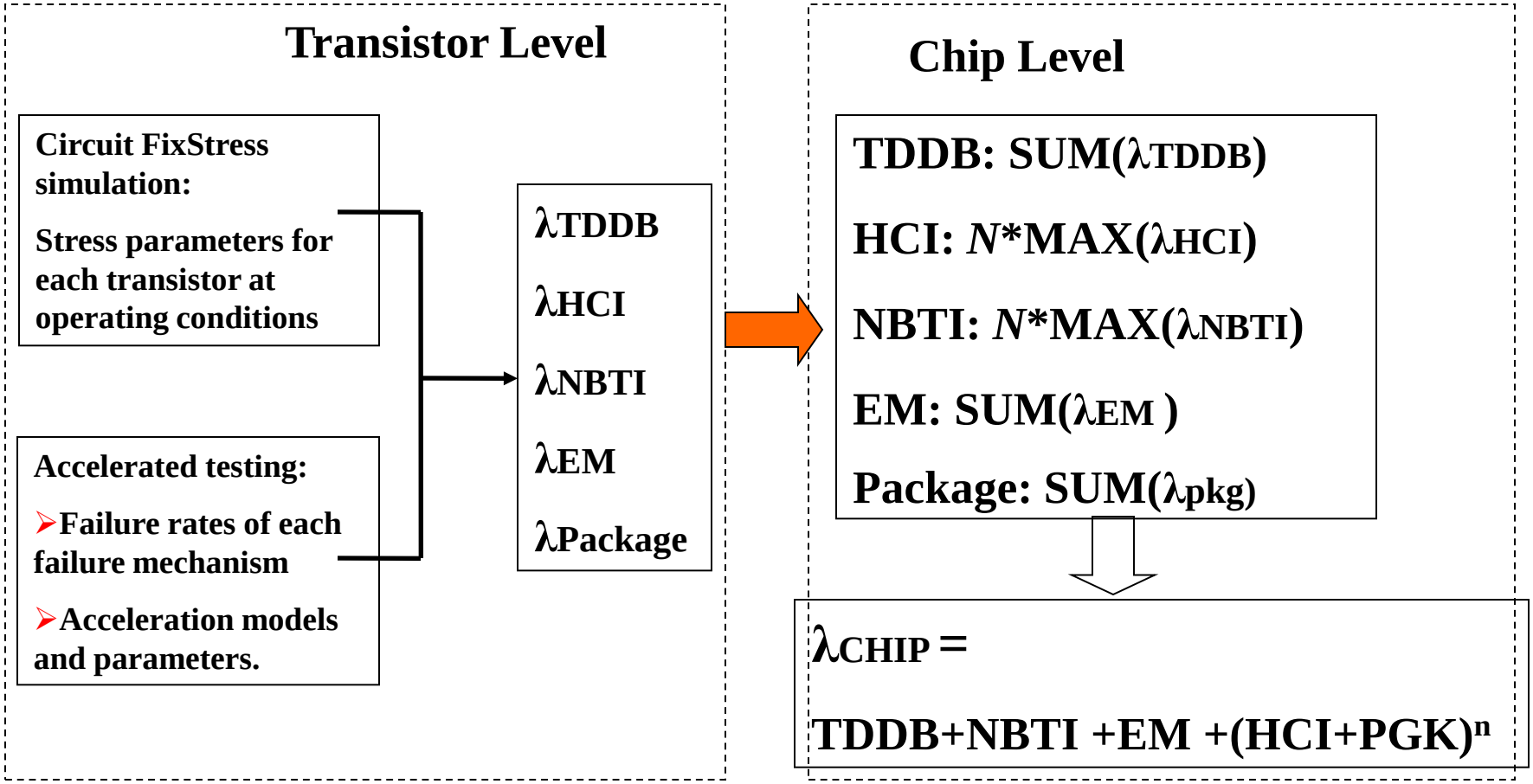
Benefit to the User !!

Believable Reliability by Design

- Customer can follow specification and believe the FIT calculation
- Customer can choose his parts based on Reliability as a Design Constraint.

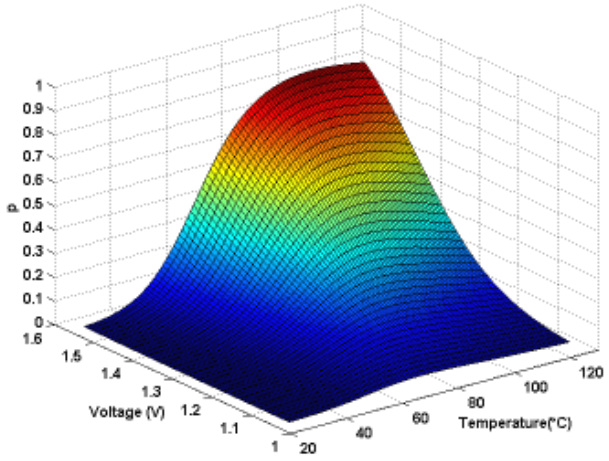

MURPHY'S LAW
Anything that can go wrong, will go wrong.
FRIENDS COME AND GO, BUT ENEMIES ACCUMULATE.
WHEN A BROKEN APPLIANCE IS DEMONSTRATED FOR THE REPAIRMAN, IT WILL WORK PERFECTLY.
THE REPAIRMAN WILL NEVER HAVE SEEN A MODEL QUITE LIKE YOURS BEFORE.
IF YOU TRY TO PLEASE EVERYBODY,
YOU WILL REMEMBER THAT
OUT THE TRASH WHEN
IF IT JAMS - FORCE IT. IF IT BREAKS, IT NEEDED REPLACING ANYWAY.
EVERYONE HAS A SCHEME FOR GETTING RICH THAT WILL NOT WORK.
YOU WILL ALWAYS FIND SOMETHING IN THE LAST PLACE YOU LOOK.
THE OTHER LINE ALWAYS MOVES FASTER.
BUILD A SYSTEM THAT EVEN A FOOL CAN USE, AND ONLY A FOOL WILL USE IT.
NO MATTER HOW LONG OR HARD YOU SHOP FOR AN ITEM, AFTER YOU'VE BOUGHT IT, IT WILL BE ON SALE SOMEWHERE CHEAPER.
NOTHING IS AS EASY AS IT LOOKS.
EVERYTHING TAKES LONGER THAN YOU THINK.
IF THERE IS A POSSIBILITY OF SEVERAL THINGS GOING WRONG, THE ONE THAT WILL CAUSE THE MOST DAMAGE WILL BE THE ONE TO GO WRONG.
COROLLARY: IF THERE IS A WORSE TIME FOR SOMETHING TO GO WRONG, IT WILL HAPPEN THEN.
ALL WARRANTIES EXPIRE UPON PAYMENT OF INVOICE.
IT IS IMPOSSIBLE TO MAKE ANYTHING FOOLPROOF BECAUSE FOOLS ARE SO INGENIOUS.
WHENEVER YOU SET OUT TO DO SOMETHING, SOMETHING ELSE MUST BE DONE FIRST.
EVERY SOLUTION BREEDS NEW PROBLEMS.
THERE IS ALWAYS ONE MORE BUG.
IF ANYTHING SIMPLY CANNOT GO WRONG, IT WILL ANYWAY.
ANYTHING GOOD IN LIFE IS EITHER ILLEGAL, IMMORAL OR FATTENING.
IF MORE THAN ONE PERSON IS RESPONSIBLE FOR A MISCALCULATION, NO ONE WILL BE AT FAULT.
BEAUTY IS ONLY SKIN DEEP, UGLY GOES TO THE BON

Failure Rate Estimation at System Level

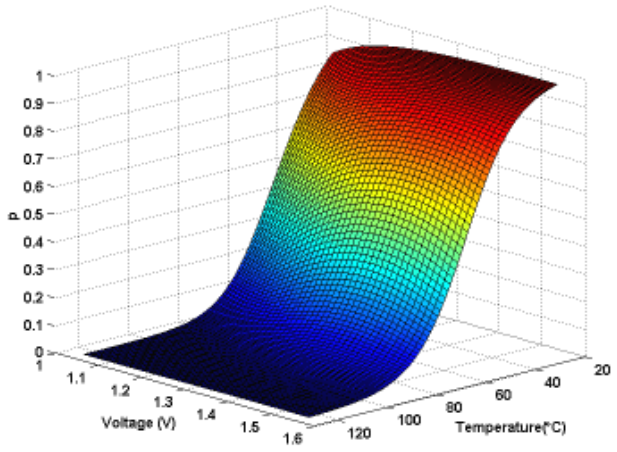


Failure Distribution at Accelerated Conditions for Multiple Mechanism Stress Validation

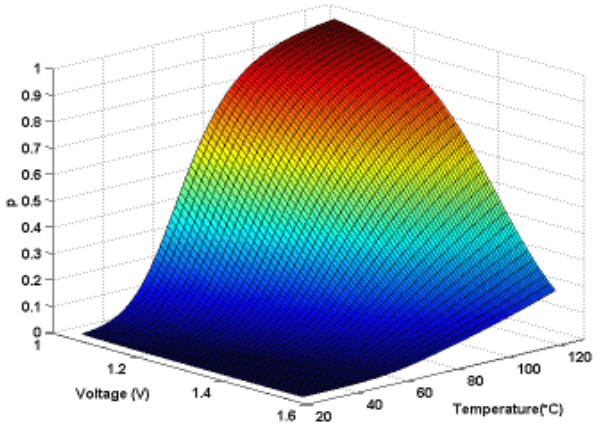
TDDB failure percentage



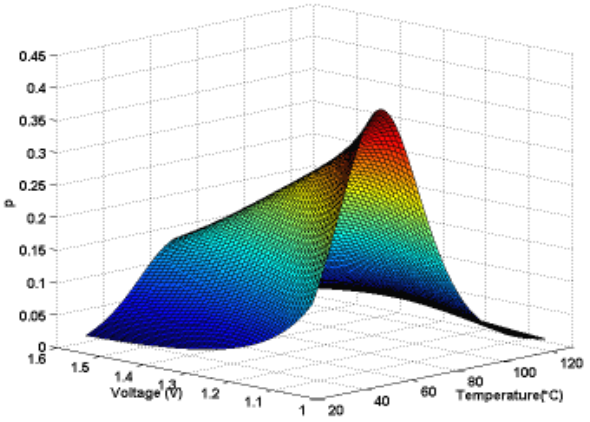
HCI failure percentage



EM failure percentage



NBTI failure percentage

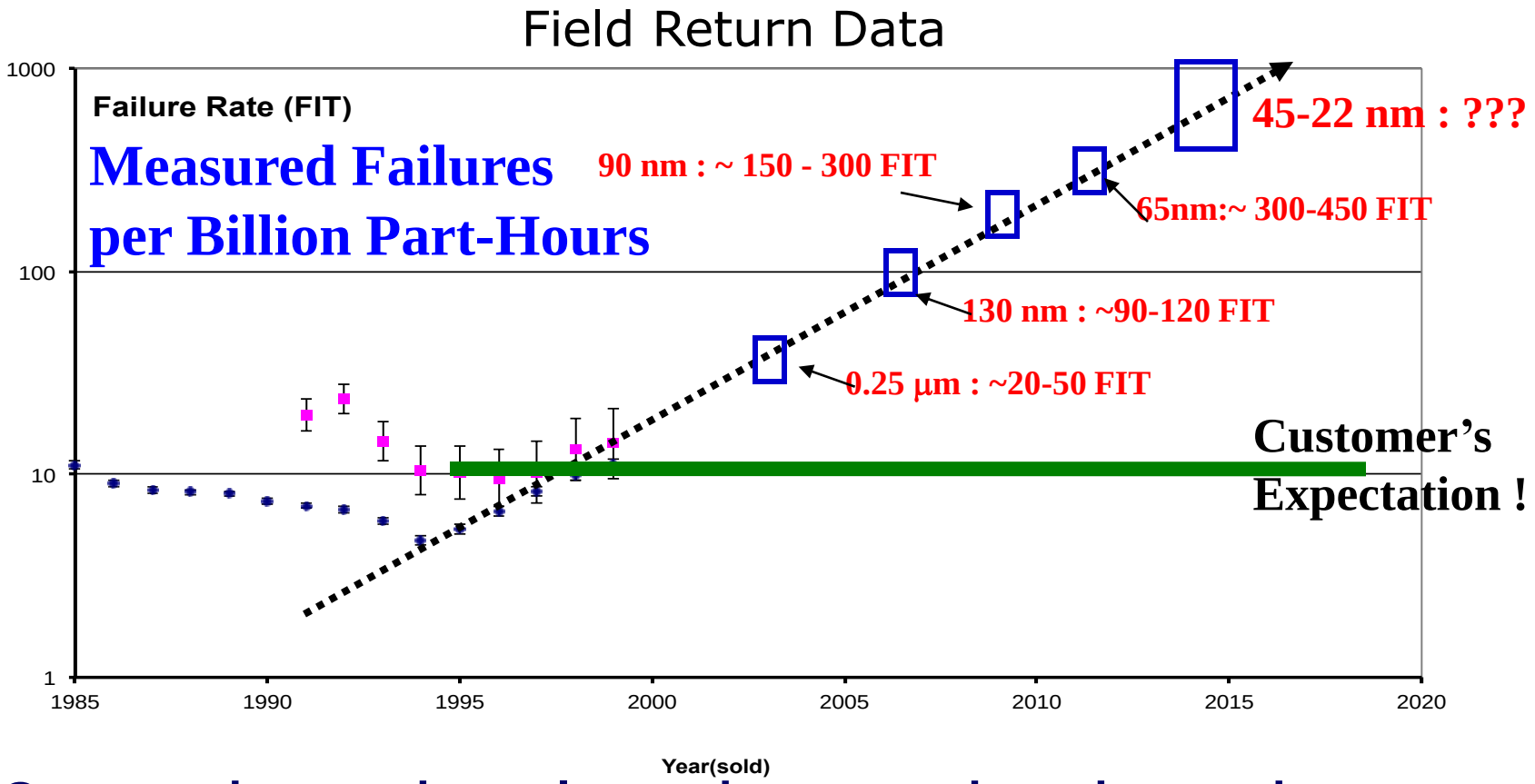


PROBLEM !!!

- Quality and Reliability of the most advanced Nano-scale electronic devices are based on outdated standards and inappropriate models
- Reported failure rate (FIT) is not a real value, yet 80% of systems continue to include a FIT model based on Telcordia/Mil-217
- Reported FIT rates OVERESTIMATE the reliability by at least 100 times (perhaps > 1000)

THIS IS A MAJOR PROBLEM FOR CONSUMERS WHO NEED OR EXPECT HIGH RELIABILITY

Field Component FIT (λ) vs. Year Produced



- Compared to previous electronic system data, the trend continues at a much greater than expected rate.
- Bernstein's Law: ~10x increase in FIT every 10 years

Multiple Failure Mechanisms

- Traditional Reliability approach fails to predict Field Failures
- Modeling, Simulation and Acceleration alone will NOT yield true results without Accurate Models
- We CAN model and PREDICT Field Failure Rates under Known Conditions with a more complete picture of the mechanisms

Reliability Engineering

- Determine how systems and processes fail
- Measure, track, and predict levels of reliability in various phases of system/process life cycle
- Improve system/process reliability by controlling failure causes
- Provide input to decision makers on how to achieve the above objectives in an optimal way

Important Interactions

- ✓ Active Circuits Flow Current
- ✓ Current gets HOT
- ✓ Heat and Current cause Degradation
- ✓ Degradations shift frequencies
- ✓ Compensation circuits burn more current
- ➢ Together: Circuits need to be modeled based on their application

System Level Expectations

- Boards are designed with acceptable FITs based on customer expectations
- These Expectations may be as high as 5000 FIT per board (all chips considered)
- 1% Failure per year ~ 1141 FIT !

Fortunately, most Customers have LOW expectations for component reliability

Qualification TODAY

Industry 'Standard' FIT (failures in time) model:

$$FIT = \frac{\#failures}{\#parts * time * AF} * 10^9$$

Acceleration Factor (AF) is the product of Voltage and Temperature acceleration factors

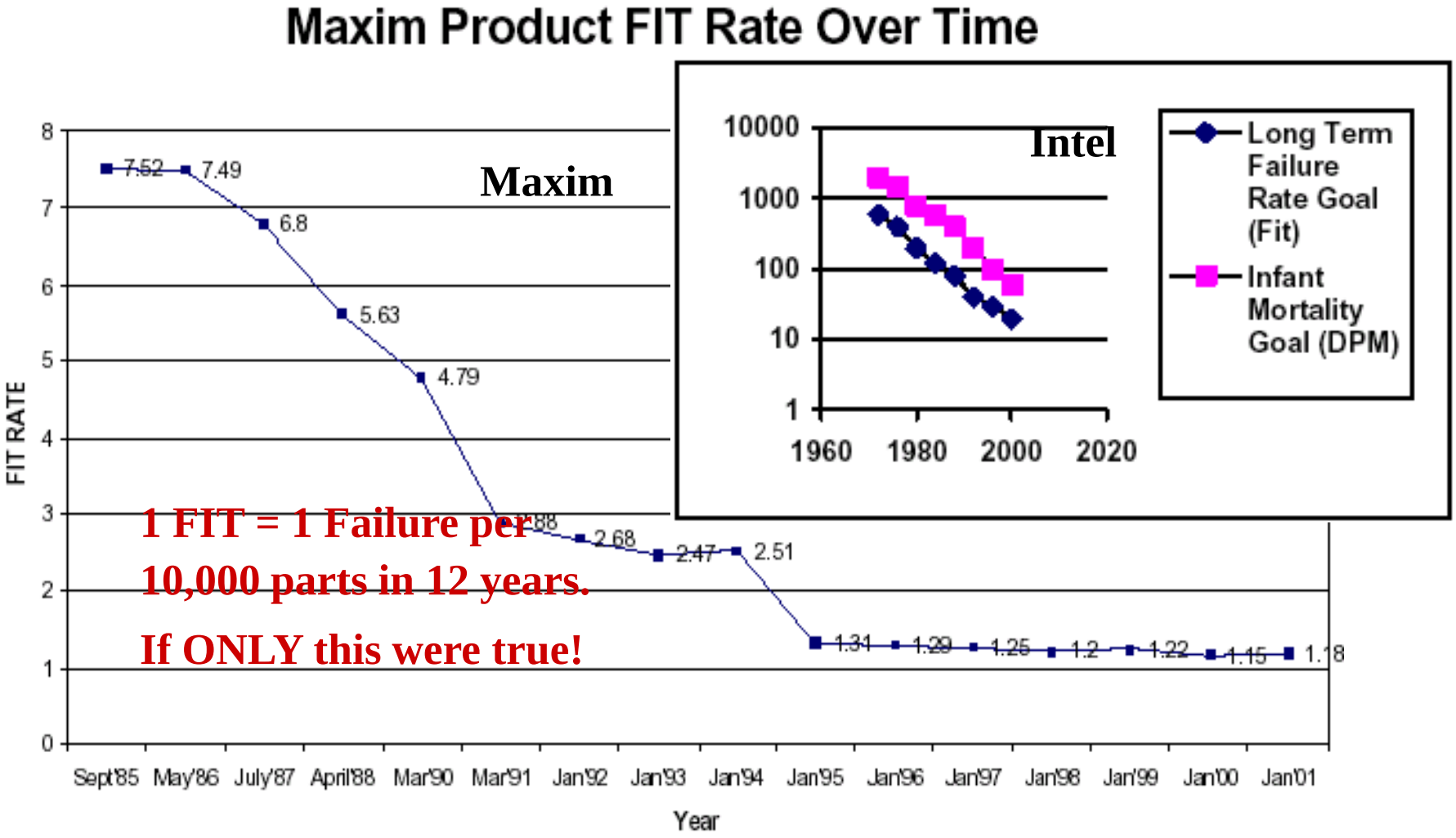
$$AF = AF_V * AF_T$$

Two KILLER problems:

1. This does NOT fit with KNOWN failure models
2. When ZERO failures are reported, there is NO statistical meaning to the acceleration factor
3. Practice is to assume 1 failure for 60% confidence

Semiconductor Industry 'Joke'

Manufacturers Claim FIT rate is decreasing as technologies advance



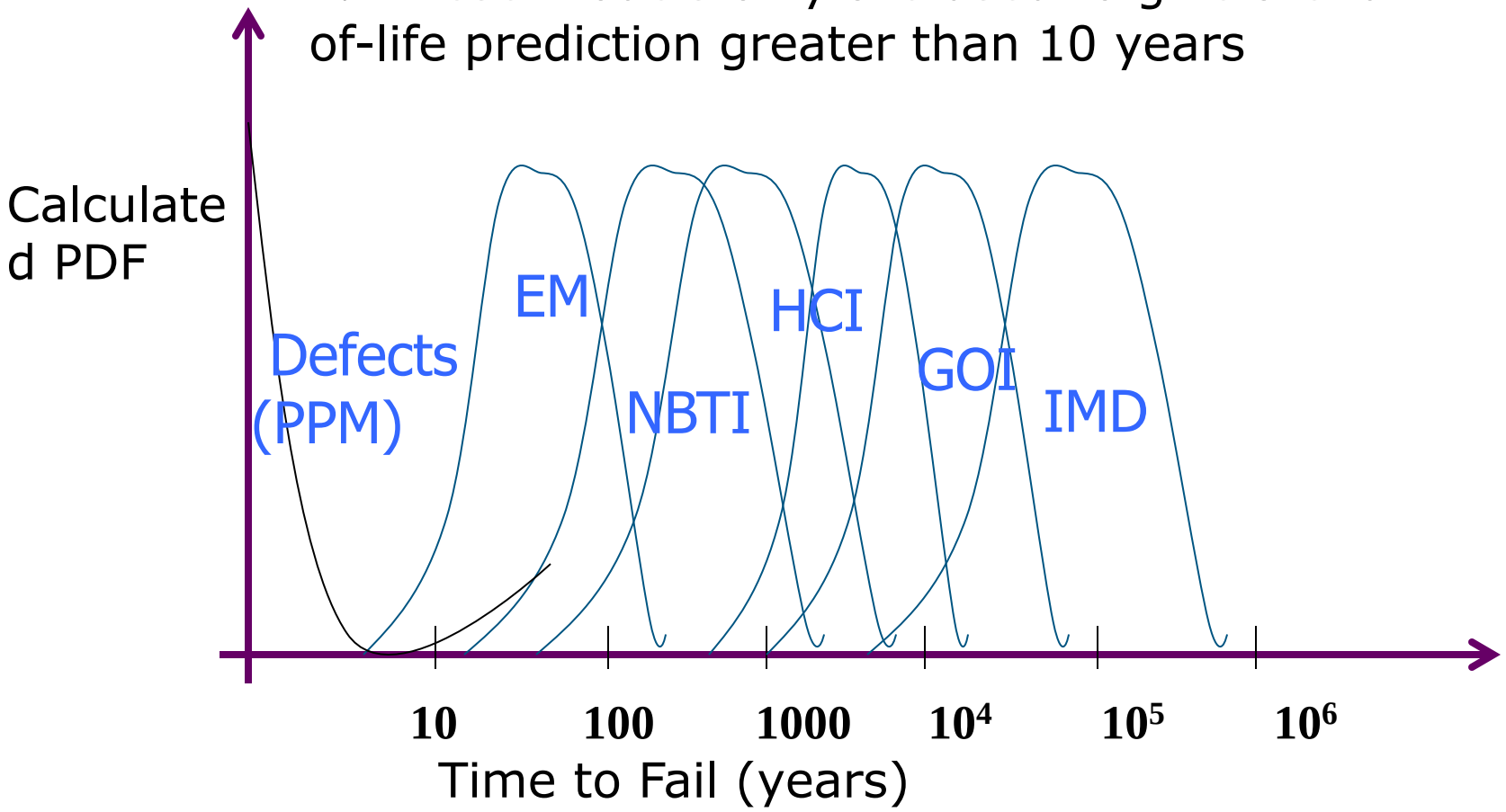
Typical Qualification Process

- Foundry's Carefully Evaluate All Known Mechanisms
- Models are placed in EDA tools to predict end of life:

40nm Process						
Input Conditions **core Vcc=1.1V, I/O Vcc=1.8V, Tjmax=110.0C. Product lifetime=10.0years.**						
	Items	**Device**	**Dimension**	**Decision**	**Result (YEARS)**	**Fail Criterion / SPEC**
Process Reliability	**GOI**	core NMOS	5E6 um^2	pass	5.89E+08	0.1% cum. fail, DC>=10 years
		core PMOS	1E7 um^2	pass	61155.12	
		I/O NMOS	1E6 um^2	pass	2.10E+08	
		I/O PMOS	1E6 um^2	pass	9.30E+08	
	HCI	core NMOS	9.0/0.036	pass	2034.13	delta Idsat>=10%, 0.1% cum. fail, AC>=10 years
		core PMOS	9.0/0.036	pass	2262.74	
		I/O NMOS	9.0/0.135	pass	3339.19	
		I/O PMOS	9.0/0.135	pass	1.03E+05	
	NBTI	core PMOS	9.0/0.036	pass	693.11	delta Idsat>=10%, 0.1% cum. fail, AC>=10 years
		I/O PMOS	9.0/0.135	pass	250.78	
	EM (DC)	M1		pass	18.74	delta R<=10%, DC>=10 years
		inter metal		pass	18.58	
		top metal		pass	266.55	
		cont		pass	113.32	
		via1-- V1M1		pass	17.59	
		via1-- V1M2		pass	17.49	
		inter via-- VxMx		pass	18.72	
		inter via-- VxMx+1		pass	18.36	
		top via-- VzMz		pass	25.73	
		top via-- VzMz+1		pass	266.55	
	IMD-TDDB	M1		pass	5.29E+06	0.1% cum. fail, DC>=10 years
		inter metal		pass	2.12E+08	
		via1-- V1M2		pass	8.04E+05	
		via1-- V1V1		pass	4.89E+06	

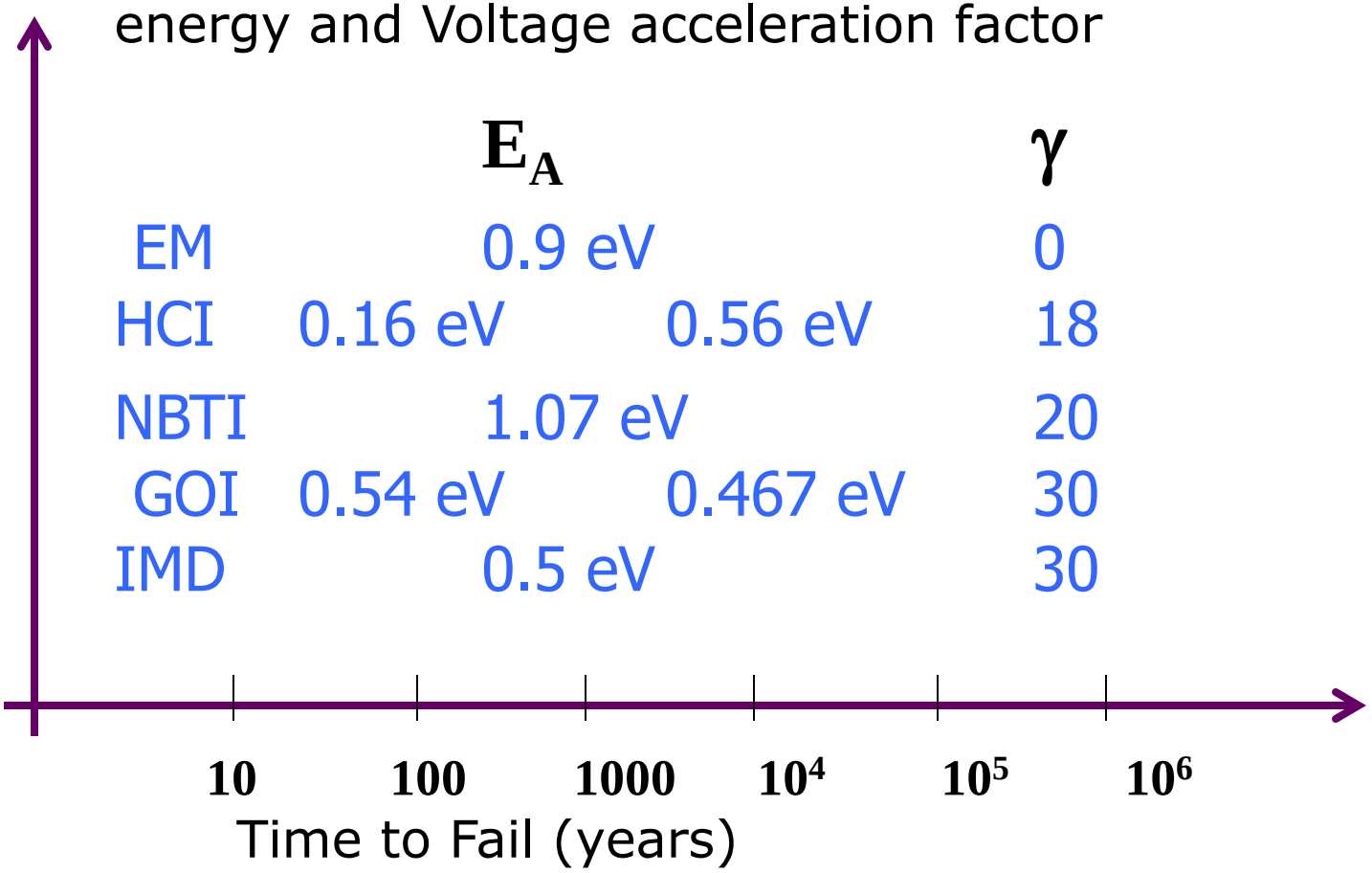
Fundamental Problem

1. These models only are used to give a end-of-life prediction greater than 10 years



Fundamental Problem

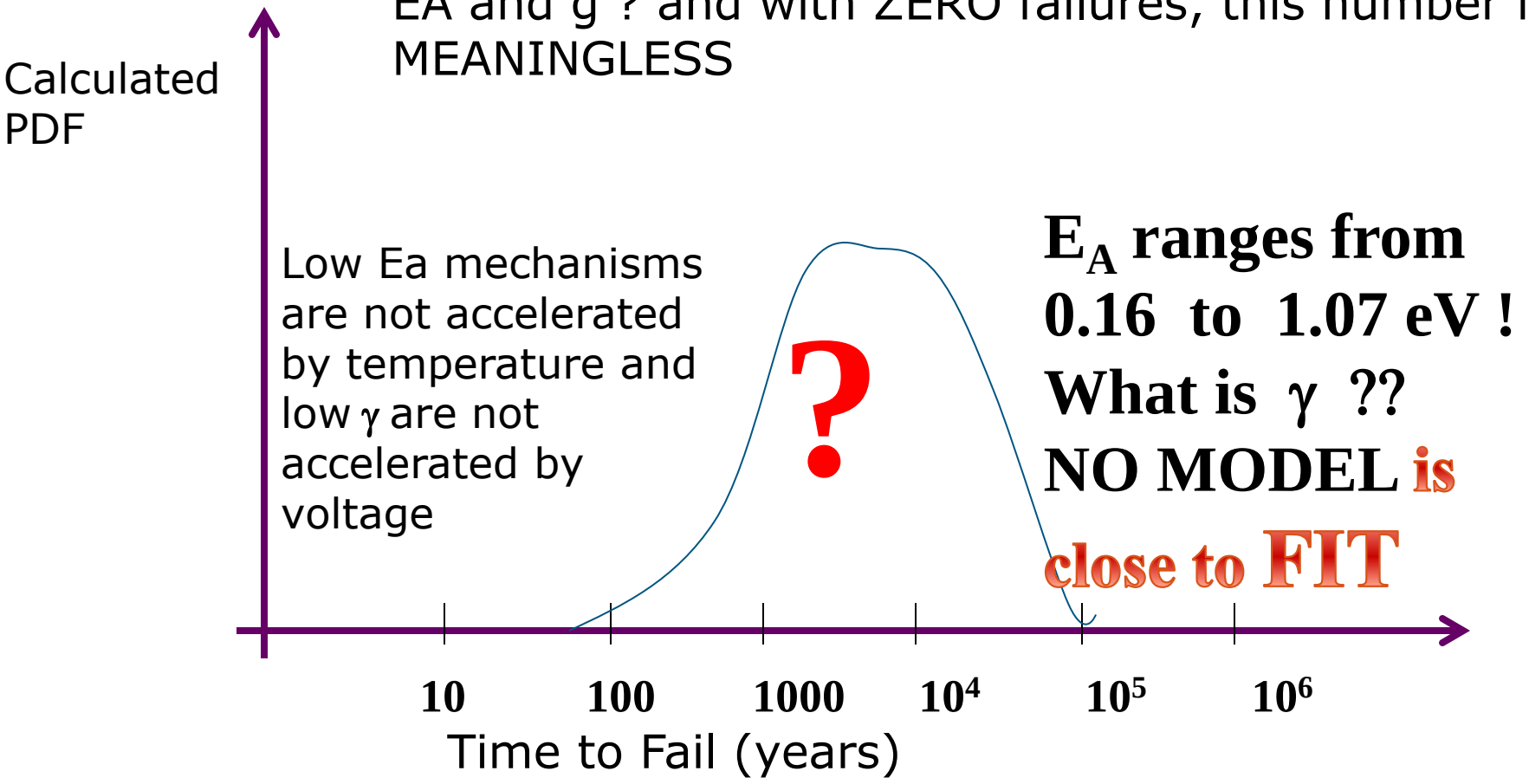
2. Each Model has a different Activation energy and Voltage acceleration factor



	E_A		γ
EM	0.9 eV		0
HCI	0.16 eV	0.56 eV	18
NBTI	1.07 eV		20
GOI	0.54 eV	0.467 eV	30
IMD	0.5 eV		30

Fundamental Problem

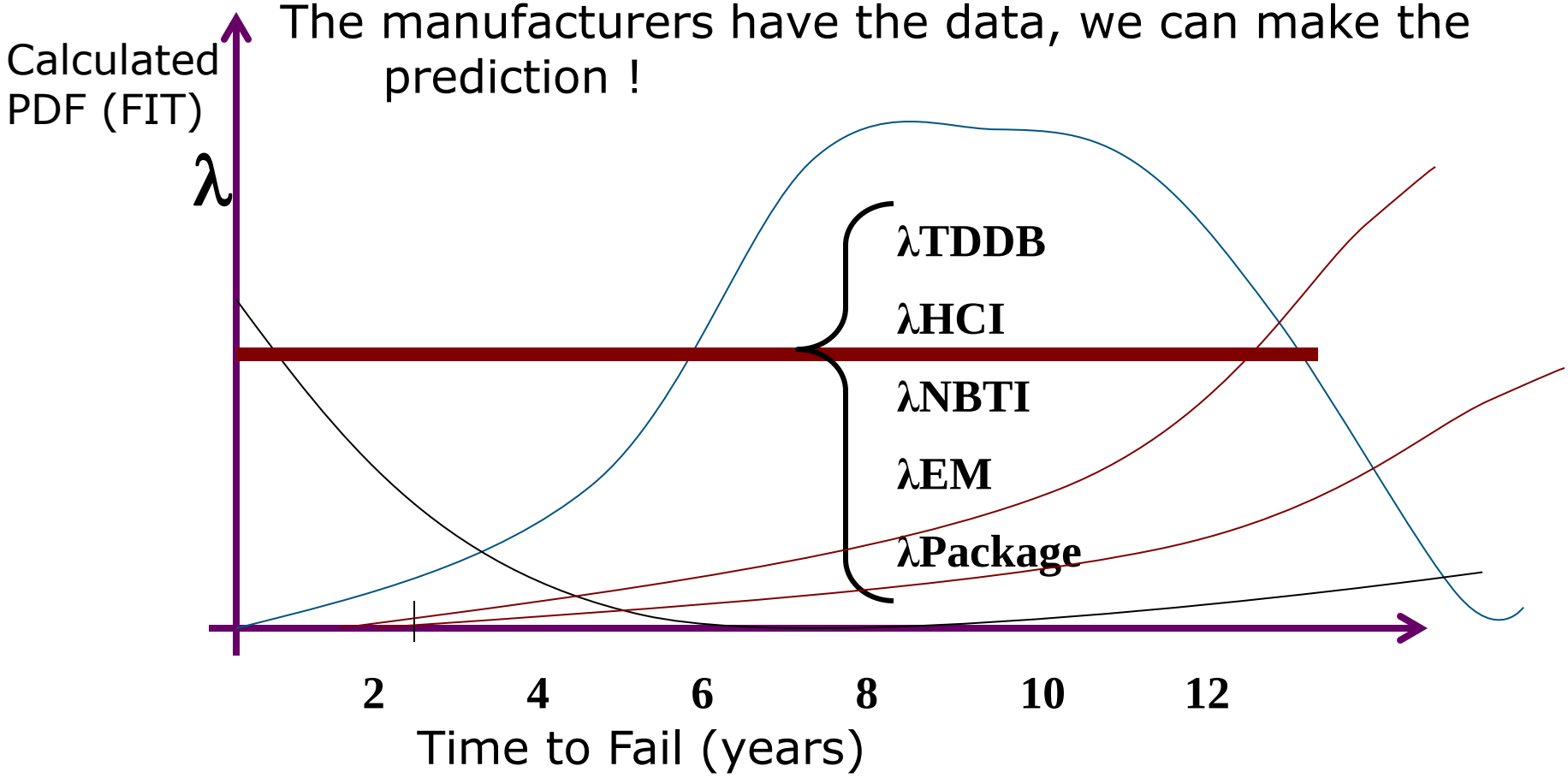
3. HTOL Test is used to calculate FIT Rate ??? Which EA and g ? and with ZERO failures, this number is MEANINGLESS



FIXtress™ : A MORE ACCURATE FIT

$$\lambda \sim \Sigma(1/MTTF_1+1/MTTF_2+\ldots+1/MTTF_n)$$

The manufacturers have the data, we can make the prediction !



Our Guiding Principle:

"It is better to be roughly right than precisely wrong"

— John Maynard Keynes

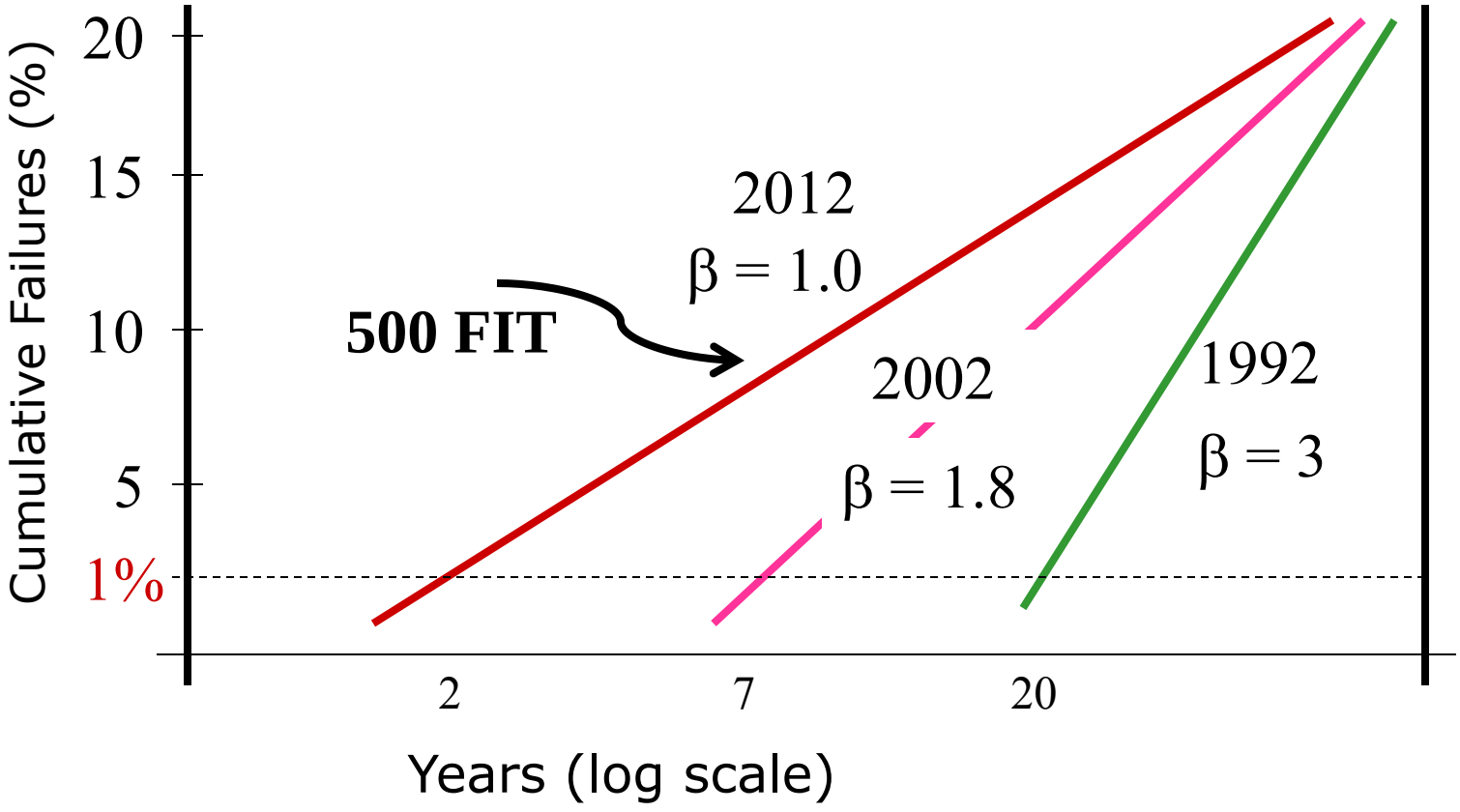


Known Wear-out Mechanisms

- Package defects: Understood, technical issues can be managed for future parts, may still be responsible for ~1/2 failures in field. Failures related to Power and Thermal cycles.
- Silicon defects: Understood, fundamental limitation on chip yield and extrinsic defects (not strongly thermally activated).
- EM, Corrosion, EOS: Mostly Understood, and is highly accelerated by Temperature and Speed. Most product lifetimes are limited by EM.
- Oxide breakdown/Hot Carrier Injection: Understood, accelerated by voltage. Technical limitations relating to SEU and Noise Margins.
- Assumption: Industry will always design for 'reasonable life' considering all these areas without any one mechanism dominating another.
- **Justifies combined failure mechanism model**
- **B –> 1, combined failure rate: $\lambda = \Sigma (\lambda_i)$: FIT rate !**

Device Failures NOW dominates System Failures

3 – Year Typical Design Life for Most Modern Components !



Multiple Mechanisms Don't Add Up !!!

- Single Mechanism Model:
  - $AF_{system} = AF_{Thermal} * AF_{Electrical}$
- BUT….Multiple Mechanisms Compete

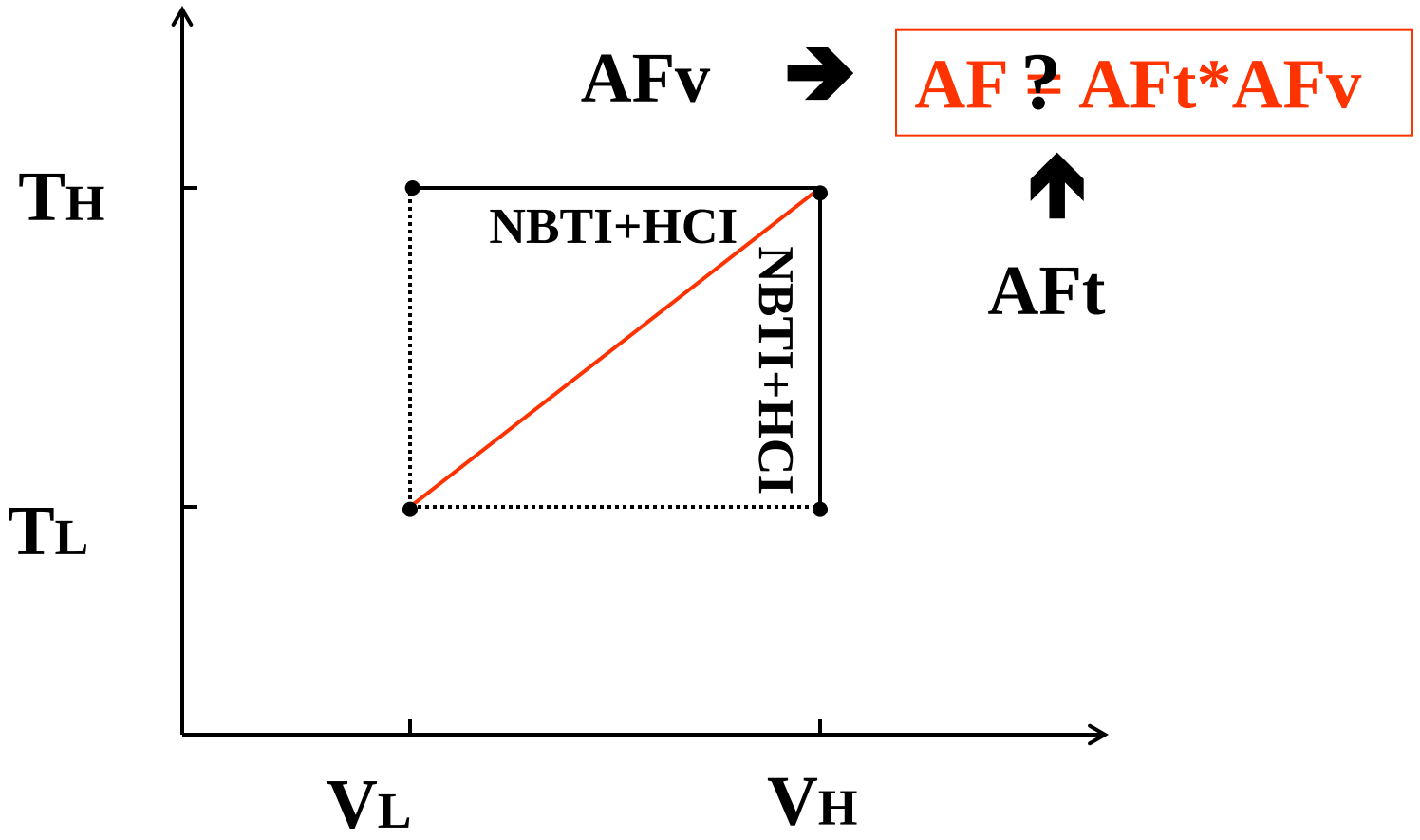
$$MTTF_{use} = MTTF_{test} * AF_{MM}$$

$$AF_{MM} = \frac{1}{\frac{1}{AF_{mech1}} + \frac{1}{AF_{mech2}}}$$

- The True acceleration factor is the SMALLER one, not the one which exposes a failure

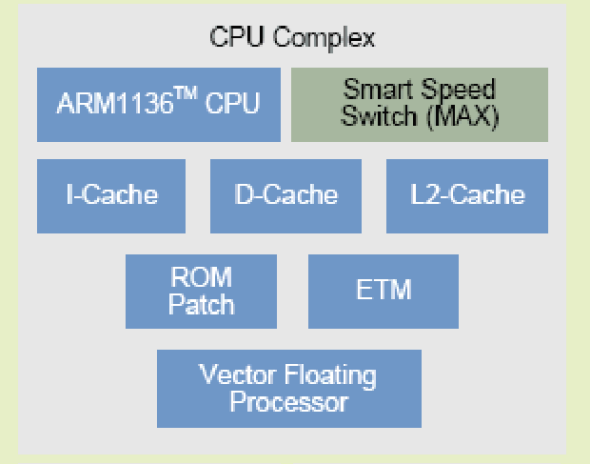
Multiple Failure Mechanisms Study

- Conventional Acceleration Factors



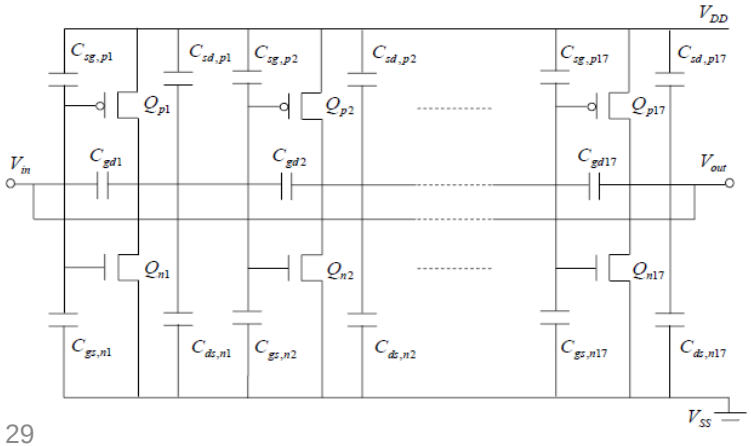
Multiple Failure Mechanisms Study - Experiment Setup

- Static Burn In - Microprocessor





- Dynamic Burn In - RO



Conclusions

- We have developed a prediction model that is based on 4 failure mechanisms
- Our model is more accurate than the single failure model currently in use
- Collaboration with Industry is Necessary to Verify our Models and to keep pace with advancing technology
- Integrating new models into fiXtress revolutionizes reliability prediction